REMARKS

The present Amendment cancels claims 1-20 and adds new claims 21-24. Therefore, the present application has pending claims 21-24.

The specification stands objected to being that the Examiner alleges that the specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The specification has been reviewed. However, Applicants were unable to uncover any such minor errors. Therefore, the Examiner is respectfully requested to identify such minor errors the Examiner may be aware of so that such errors can be immediately corrected to expedite prosecution of the present application.

The Abstract of the disclosure stands objected to due to various informalities noted by the Examiner in paragraph 5 of the Office Action. Various amendments were made throughout the Abstract to correct the informalities noted by the Examiner and to bring it into conformity with the requirements of MPEP §608.01(b).

The title of the invention stands objected to as not being descriptive of the invention. The title of the invention was changed to "PARALLEL PROCESSING DEVICE FOR IMAGE DATA WITH SIMD ALU" which Applicants submit is descriptive of the present invention. Also, it should be noted that this title was suggested by the Examiner. Therefore, this objection is overcome and should be withdrawn.

Claims 2, 7, 9, 15-17, 19 and 20 stand objected to due to informalities noted by the Examiner in paragraph 7 of the Office Action, claims 8, 9 and 11-13 stand rejected under §112, first paragraph, claims 1-9, 11, 12 and 18-20 stand rejected

under §112, second paragraph, claims 1-8, 10-12 and 14-20 stand rejected under 35 USC §102(e) as being anticipated by Morton (U.S. Patent No. 5,822,606), and claims 9 and 13 stand rejected under 35 USC §103(a) as being unpatentable over Morton in view of Horishi (U.S. Patent No. 6,115,073). As indicated above, claims 1-20 were canceled. Therefore, these objections and rejections of claims 1-20 are rendered moot. Accordingly, reconsideration and withdrawal of the above noted objections to claims 1-20 and rejections of claims 1-20 is respectfully requested.

It should be noted that the cancellation of claims 1-20 was not intended nor should it be considered as an agreement on Applicants part that the features recited in claims 1-20 are taught or suggested by any of the references of record whether taken individually or in combination with each other. The cancellation of claims 1-20 was simply intended to expedite prosecution of the present application.

As indicated above, the present Amendment adds new claims 21-24 directed to a data processor and a data processing unit. The data processor includes a central processing unit (CPU) which fetches an instruction, decodes the instructions and executes the instruction, a first data bus coupled to the CPU, an arithmetic and logic unit which operates to perform an arithmetic operation, a memory unit which stores results of the arithmetic operation performed by the arithmetic and logic unit, a second bus coupled to the arithmetic and logic unit and the memory unit and an address bus coupled to the CPU, the arithmetic and logic unit and the memory unit.

According to the present invention, a bit width of the second bus is wider than a bit width of the first bus, the central processing unit provides a plurality of control signals to the arithmetic and logic unit in response to a result of decoding a first

instruction to control the arithmetic and logic unit and the arithmetic and logic unit is provided data from the memory unit via the second bus and is capable of operating a plurality of arithmetic operations using the data according to the control signals related to the first instructions.

The data processing unit includes elements similar to that recited with respect to the data processor with the exception that the arithmetic and logic unit is a single instruction multiple data (SIMD) arithmetic logic unit.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention now more clearly recited in new claims 21-24 are not taught or suggested by Morton or Horishi whether taken individually or in combination with each other as suggested by the Examiner.

Particularly, both Morton and Horishi fails to teach or suggest a CPU which fetches an instruction, decodes the instruction and executes the instruction and an arithmetic and logic unit which operates to perform an arithmetic operation such that a bit width of a second data bus coupled to the arithmetic and logic unit and a memory unit is wider than a bit width of a first data bus coupled to the CPU and that the CPU provides a plurality of control signals to the arithmetic logic unit in response to the result of decoding a first instruction to control the arithmetic logic unit as in the present invention.

Even further, both Morton and Horishi fail to teach or suggest that the arithmetic and logic unit is provided data from the memory unit via the second data

bus and is capable of operating a plurality of the arithmetic operations using the data according to the control signals related to the first instruction as in the present invention.

Thus, the features of the present invention as now more clearly recited in new claims 21-24 are not taught or suggested by any of the references of record whether taken individually or in combination with each other.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-20.

In view of the foregoing amendments and remarks, Applicants submit that claims 21-24 are in condition for allowance. Accordingly, early allowance of claims 21-24 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (520.40265X00).

Respectfully submitted,

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